

REMARKS

Claims 1-15 are pending in the application. The status of the application and claims is as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
Title	Objection	<ul style="list-style-type: none">• Non-descriptive title
6-8	Objection	<ul style="list-style-type: none">• Dependency from higher numbered claim
15	Objection	<ul style="list-style-type: none">• Dependent upon a rejected base claim, but otherwise allowable
7	§112, second paragraph	<ul style="list-style-type: none">• Lack of antecedent basis for "multiplexer", but otherwise allowable
1-6, 8-14	§102(e) Anticipation	<ul style="list-style-type: none">• Pawlowski (U.S. Patent No. 5,787,475).

5 Applicant thanks the Examiner for indicating the allowability of claims 7 and 15. Applicant has amended the title and claims 6-8 in accordance with the Examiner's suggestions, and has also provided discussion for distinguishing the present invention from the art cited against it.

OBJECTION TO THE TITLE

10 1. *Applicant has replaced the title with one believed to be more specific.*

Applicant believes him that the new title is now adequately descriptive. However, if this title remains not descriptive, the Examiner is invited to provide recommendations .

OBJECTIONS TO CLAIMS 6-8

15 2. *Applicant has renumbered in the claims in accordance with the suggestion of the Examiner.*

Applicant thanks the Examiner for pointing out this informality.

35 U.S.C. §112, SECOND PARAGRAPH INDEFINITENESS OF CLAIM 7

3. *Applicant has corrected claim 7 to correctly read "a multiplexer".*

5 **35 U.S.C. §102(e), CLAIMS 1-6 AND 8-14 ANTICIPATION BY PAWLOWSKI**

4. *Pawlowski does not anticipate the present invention because the device of Pawlowski, in response to a data output request, outputs an amount of data that corresponds to the amount of data that can be stored between neighboring output start addresses, and does not output an amount of data*
10 *greater than the amount of data that can be stored between neighboring output start addresses.*

The last element of claim one requires that the data storage device is configured such that:

[the] selectable output start addresses are spaced from one another such
15 that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request

Or, stated another way, when a data output request is provided to the device, it can output an amount of data larger than the amount between
20 neighboring output start addresses that the device can be addressed by.

This is not the way that Pawlowski operates. In Pawlowski, the main memory 14 is segmented into a plurality of addressable cache lines 18 (4/55-56). If another system component (e.g., the I/O module 24) wants to read out data

stored in the main memory 14, it has to address the main memory 14 using the start address of one of the cache lines 18, and will receive the contents of a complete cache line (see, e.g., 6/15-19 and 50-59).

Therefore, the main memory 14 of Pawlowski is a data storage device 5 comprising the feature that the selectable output start addresses are spaced from one another such that the amount of data that can be stored between neighboring output start address corresponds to the amount of data output in response to a data output request.

Pawlowski does not permit the access of the data storage device in 10 amounts other than entire cache lines. According to Pawlowski, "All data transfers over the system bus must generally comprise an entire cache line worth of data." 4/59-60. Since the addressability of the cache memory 14 is only permitted at the beginning of the cache lines, it is only possible, according to Pawlowski, to get an amount of data equal to the spacing between neighboring 15 start addresses per each request. In the relevant portions cited by the Examiner, e.g., 7/15-25, a "prefetch" of data beyond a single cache line may be performed, but this involves making a second or multiple requests of the memory: "... the data retriever may request a next consecutive cache line of data from main memory if the I/O controller has directed a second prefetch." 7/58-60.

20 The present invention primarily permits an overlap of the memory regions that can be retrieved based on the output start addresses of the memory device—i.e., multiple requests of the device may not be required when accessing

an amount of memory larger than the spacing of the possible output start addresses.

Similarly, independent claim 9 requires the outputting of stored data from the data storage device that is greater in quantity than the space between the 5 neighboring output start addresses. Since Pawlowski only puts out a single cache line, and the neighboring output start addresses begin at the start of each cache line, Pawlowski does not anticipate independent claim 9 of the application.


All remaining claims in the application depend from either claim 1 or claim 9, and therefore are not anticipated by Pawlowski.

10 For these reasons, the Applicant asserts that the claim language clearly distinguishes over the prior art, and respectfully request that the Examiner withdraw the §102(e) rejection from the present application.

CONCLUSION

Inasmuch as each of the objections have been overcome by the amendments, and all of the Examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered, the rejections be withdrawn and that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 26, 2003.



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